CLAIMS:

1. In a switching system comprising:

a switch;

a plurality of input interfaces each connected to input ports of the switch, each of the input interfaces including a scrambler using a predetermined pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to a corresponding input port of the switch; and

a plurality of output interfaces each connected to output ports of the switch, each of the output interfaces including a descrambler using the predetermined pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from a corresponding output port of the switch to output frames of original data,

a scramble control method comprising the steps of:

resetting the scramblers simultaneously; and

resetting the descramblers simultaneously.

2. The scramble control method according to claim 1, wherein the scramblers and the descramblers operate according to a predetermined system clock, wherein

the scramblers are simultaneously initialized at a first time point and thereafter are not reset, and

the descramblers are simultaneously initialized at a second time point and thereafter are not reset, wherein the second time point is delayed from the first time point by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

3. The scramble control method according to claim 2, wherein the first time point is a time when the switching system starts up.

4. The scramble control method according to claim 1, wherein the scramblers and descramblers are of frame synchronizing type.

5. The scramble control method according to claim 4, wherein a cycle of a pseudorandom pattern generated by the predetermined pseudorandom pattern generator is set to be longer than a length of the frame.

6. The scramble control method according to claim 5, wherein the predetermined pseudorandom pattern generator uses a generator polynomial: $1 + X^{43}$.

7. The scramble control method according to claim 1, further comprising the steps of:

generating a scrambler state indicating a

pseudorandom pattern generated by the predetermined pseudorandom pattern generator at predetermined intervals;

sending the scrambler state to the scramblers so that the scramblers are simultaneously reset to the pseudorandom pattern indicated by the scrambler state; and

sending the scrambler state to the descramblers with a delay of a time period required for transferring a frame from an input interface to an appropriate output interface through the switch, so that the descramblers are simultaneously reset to the pseudorandom pattern indicated by the scrambler state.

8. The scramble control method according to claim 7, wherein the scramblers and descramblers are of frame synchronizing type.

9. The scramble control method according to claim 8, wherein a cycle of a pseudorandom pattern generated by the predetermined pseudorandom pattern generator is set to be longer than a length of the frame.

10. The scramble control method according to claim 9, wherein the predetermined pseudorandom pattern generator uses a generator polynomial: $1 + X^{43}$.

11. In a switching system comprising:

a switch;

a plurality of input interfaces each connected to input ports of the switch, each of the input interfaces including a scrambler using a predetermined pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to a corresponding input port of the switch; and

a plurality of output interfaces each connected to output ports of the switch, each of the output interfaces including a descrambler using the predetermined pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from a corresponding output port of the switch to output frames of original data,

a scramble control method comprising the steps of:

at each of the scramblers,

generating a scrambler state indicating a pseudorandom pattern generated by the predetermined pseudorandom pattern generator in frame timing;

assembling a frame including the scrambler state;

transferring the frame including the scrambler state to the switch;

at each of the descramblers,

receiving a frame including a scrambler state;

resetting the predetermined pseudorandom pattern generator to the pseudorandom pattern indicated by the scrambler state.

12. The scramble control method according to claim 11, wherein the scramblers and descramblers are of self-synchronizing type.

13. The scramble control method according to claim 11, wherein the scramblers and descramblers are of frame synchronizing type.

14. The scramble control method according to claim 11, wherein a cycle of a pseudorandom pattern generated by the predetermined pseudorandom pattern generator is set to be longer than a length of the frame.

15. The scramble control method according to claim 14, wherein the predetermined pseudorandom pattern generator uses a generator polynomial: $1 + X^{43}$.

16. A switching system comprising:

a switch;

a plurality of input interfaces each connected to input ports of the switch, each of the input interfaces including a scrambler using a predetermined pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to a corresponding input port of the switch;

a plurality of output interfaces each connected to output ports of the switch, each of the output interfaces including a descrambler using the predetermined pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from a corresponding output port of the switch to output frames of original data; and

a reset pulse generator for generating a scrambler reset pulse and a descrambler reset pulse, wherein the scrambler reset pulse is sent to all the scramblers at equal timing, and the descrambler reset pulse is sent to all the descramblers at equal timing.

17. The switching system according to claim 16, wherein the scramblers and the descramblers operate according to a predetermined system clock, wherein

the scramblers are initialized in response to the scrambler reset pulse and thereafter are not reset, and

the descramblers are initialized in response to the descrambler reset pulse and thereafter are not reset, wherein the descrambler reset pulse is delayed from the scrambler reset pulse by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

18. A switching system comprising:

a switch;

a plurality of input interfaces each connected to input ports of the switch, each of the input interfaces including a scrambler using a predetermined pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to a corresponding input port of the switch;

a plurality of output interfaces each connected to output ports of the switch, each of the output interfaces including a descrambler using the predetermined pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from a corresponding output port of the switch to output frames of original data; and

a scramble state generator for generating a scrambler state indicating a pseudorandom pattern generated by the predetermined pseudorandom pattern generator at predetermined intervals, wherein

the scrambler state is sent to the scramblers so that the scramblers are simultaneously reset to the pseudorandom pattern indicated by the scrambler state, and

the scrambler state is sent to the descramblers with a delay of a time period required for transferring a frame from an input interface to an appropriate output interface through the switch, so that the descramblers are simultaneously reset to the pseudorandom pattern indicated by the scrambler state.

19. A switching system comprising:

a switch;

a plurality of input interfaces each connected to input ports of the switch, each of the input interfaces including a scrambler using a predetermined pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to a corresponding input port of the switch; and

a plurality of output interfaces each connected to output ports of the switch, each of the output interfaces including a descrambler using the predetermined pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from a corresponding output port of the switch to output frames of original data,

wherein each of the scramblers further comprises:

a scramble state generator for generating a scrambler state indicating a pseudorandom pattern generated by the predetermined pseudorandom pattern generator in frame timing; and

an assembler for assembling a frame including the scrambler state, and

each of the descramblers further comprises:

a reset circuit for resetting the predetermined pseudorandom pattern generator to the pseudorandom pattern indicated by a scrambler state included in a frame received from the switch.